Amendments to the Claims

This listing will replace all prior versions, and listing, of claims in the application.

Claims 1-24. (cancelled)

25. (currently amended) A multilevel interconnect structure, comprising:

a semiconductor surface that has been provided with metal points of electrical contact ~~in said surface~~, thereover having been created a low k compound layer of inter metal dielectric comprising:

(1) a first layer of dielectric deposited on said semiconductor surface, said first layer of dielectric ~~containing~~ comprising a first network of trenches filled with air;

(2) a second layer of dielectric deposited on and in contact with said first layer of dielectric ~~on said semiconductor surface~~, said second layer of dielectric ~~containing~~ comprising a second network of trenches filled with air, ~~whereby~~ said second network of trenches ~~is~~ being in ~~physical~~ contact with and ~~intersects~~ intersecting with

said first network of trenches to form an interconnected network of trenches filled with air~~under an angle~~; and

(3) a layer of oxide deposited over said second layer of dielectric, said layer of oxide comprising:

(i) a first layer of oxide having openings created there-through, said openings being aligned with the intersections between said first and second network of trenches, enabling creation of said first and second network of trenches; and

(ii) a second layer of oxide, said second layer of oxide closing the openings in the first layer of oxide.

26. (currently amended) The multilevel interconnect structure of claim 25, ~~whereby furthermore~~ additionally a network of metal interconnects ~~interconnect lines~~ ~~is created on~~ having been created over said three layers of dielectric ~~said layer of oxide~~.

27. (currently amended) The multilevel interconnect structure of claim 25, ~~whereby furthermore~~ said layer of oxide deposited over said second layer of dielectric ~~trenches is extended in~~ having a thickness between about 1000 and 4000 Angstroms.

28. (currently amended) The multilevel interconnect structure of claim 27 whereby furthermore a network of metal interconnect lines is created on said layer of oxide deposited over said second layer of dielectric ~~extended layer of oxide~~.

Amendments to the Claims

This listing will replace all prior versions, and listing, of claims in the application.

1. (cancelled) A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate whereby the surface of said semiconductor substrate has been provided with points of electrical contact;

forming a first network of nitride filled trenches in a first level of dielectric said first level of dielectric having been deposited on the surface of said substrate;

forming a second network of nitride filled trenches in a second level of dielectric said second level of dielectric having been deposited on the surface of said first level of dielectric whereby furthermore said second network of nitride filled trenches is in physical contact with and intersects with said first network of nitride filled trenches;

depositing a first thin layer of oxide over the surface of said second layer of dielectric;

etching openings in said first thin layer of oxide said openings to align with said intersects between said first